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EXAMINER
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MATTIS, JASON E

ART UNIT	PAPER NUMBER
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2665

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DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/769,929

Applicant(s)

NANDURI ET AL.

Examiner

Jason E Mattis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 6/25/01 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because of the following informalities:

On page 5 lines 6-7 of the detailed description state that the like numbers in Figures 2 and 3 identify like elements; however no numerals are used in Figure 3 to describe any of the items. Further, page 5 of the detailed description refers to item number 104a located in Figure 3. No label 104a is found in Figure 3. It is recommended that item numbers be added to the current Figure 3.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Sang et al. (U.S. Pat. 6577636).

**With respect to claim 1, Sang et al. discloses a switch router circuit (See column 4 lines 33-46 and item 12 in Figure 2 of Sang et al. for reference to a multi-port switch 12). Sang et al. also discloses a plurality of Media Access Control units (See column 4 lines 33-46 and items 20 in Figures 1 and 2 of Sang et al. for reference to media access control units 20). Sang et al. further discloses each MAC unit connected to a data bus for receiving incoming data packets from the data bus (See Figure 2 of Sang et al. for reference to data bus 69 being connected to each of the 12 MAC units, which are represented by item number 20). Sang et al. also discloses each incoming data packet including a packet header and a packet payload,**

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with the packet header identifying a destination port to which the packet payload is to be transferred (**See column 5 lines 28-31 of Sang et al. for reference to a unit that “snoops” a data bus to determine the header information of a received packet including destination address information, which means that the packets must have a head with a destination address that identifies a destination port to which the payload is to be transferred to**). Sang et al. further discloses a controller connected to the MAC units to received the incoming packets therefrom (**See column 4 lines 33-46 and item 40 in Figure 2 of Sang et al. for reference to decision making engine 40 that is connected to the MAC units via bus 69 to receive incoming packets**). Sang et al. also discloses for each incoming data packet the controller separating the packet header of the data packet from the packet payload of the data packet (**See column 5 lines 28-52 of Sang et al. for reference to IRC 40 separating the data packet head from the data packet payload**). Sang et al. further discloses a lookup table connected to the controller to receive packet headers therefrom (**See column 14 lines 15-31 of Sang et al. for reference to IRC 40 including an address table 82**). Sang et al. also discloses that the lookup table utilizes a packet header to determine whether the destination port identified by the packet header is included within the plurality of MAC units of the switch router circuit (**See column 17 lines 19-42 of Sang et al. for reference to IRC 40 using the packet header and the address table 82 to determine which output port to forward the packet, which means that it determines if the destination port is one of the MAC units of the switch and routes the packet to the destination port**). Sang et al. further discloses a multi-port

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store/switch memory array connected to receive packet payloads of incoming data packets (**See column 4 lines 47-63 and Figures 1 and 2 of Sang et al. for reference an external memory 36**). Sang et al. also discloses that the multi-port store/switch memory array includes a plurality of storage areas with each storage areas being associated with a corresponding MAC unit such that a packet payload of an incoming data packet received by the MAC unit is stored in the corresponding storage area of the multi-port store/switch memory array (**See column 6 lines 54-67 of Sang et al. for reference to packets received by the MAC modules being sent to a store area in the external memory 36 and for reference to each of the storage areas of the external memory being associated with each of the MAC modules using frame pointers, which link a MAC unit to the area in which a received packet has been stored in the external memory 36**). Sang et al. further discloses an arbitrator connected to the multi-port store/switch memory array (**See column 4 lines 33-46 and item 42 in Figure 2 of Sang et al. for reference to a switching subsystem 42, which acts as an arbitrator, connected to the external memory 36 through bus 69**). Sang et al. also discloses that the arbitrator, in the event that the destination port identified by the packet header of an incoming data packet is included within the plurality of MAC units of the switch/router circuit, arbitrates direct connection of the memory array storage area associated with the MAC unit that receives the incoming data packet to the MAC unit identified as the destination port, thereby facilitating direct transfer of the packet payload of the incoming data packet to the destination port (**See column 5 line 53 to column 6 line 12 of Sang et al. for reference to the switch subsystem 42**

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**providing arbitrating a direct connection to send the packet payload from the external memory 36 to the transmit FIFO memory of the corresponding identified destination port or ports, meaning that the switch subsystem 42 facilitates a direct connection of the packet payload from the associated memory location of the MAC that received the packet to the transmit FIFO memory corresponding to the destination MAC port).**

**With respect to claim 2, Sang et al. discloses that each of the storage areas in the multi-port store/switch memory array includes a plurality of pass gates, one pass gate being associated with a corresponding one of the MAC units (See column 6 line 54 to column 8 line 12 and Figure 3 of Sang et al. for reference to the method by which the memory is accessed using pointers that are associated with corresponding MAC units to access specific memory areas, which means there must be a pass gate associated with each memory area so that the data may be transferred by each memory area a corresponding destination area). Sang et al. further discloses each of the plurality of storage areas further including a storage element such that the arbitrator arbitrates the pass gates of the incoming storage area to the pass gates of the outgoing storage area whereby the packet payload is transferred directly from the data storage element of the incoming storage area to the data storage element of the outgoing storage area (See column 7 line 51 to column 8 line 12 and Figure 3 of Sang et al. for reference to the elements of switching element 42 facilitating the transfer of a data payload from the external memory 36 to a transmit FIFO, which is a memory corresponding with the destination**

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**address of the payload, such that there is a direct transfer of the payload from the incoming memory location in the external memory 36 to the outgoing transmit FIFO memory area of the destination MAC port).**

**With respect to claim 3, Sang et al. discloses that the arbitrator arbitrates direct connection of the memory array storage area associated with the MAC unit that receives the incoming data packet to multiple MAC units identified as destination ports, thereby facilitating multicasting of the packet payload to multiple destination ports (See column 6 line 54 to column 8 line 26 and Figure 3 of Sang et al. for reference to the elements of switching element 42 facilitating the transfer of a data payload from the external memory 36 to a transmit FIFO, which is a memory corresponding with the destination address of the payload, such that there is a direct transfer of the payload from the incoming memory location in the external memory 36 to the outgoing transmit FIFO memory area of the destination MAC port and for further reference to a multicopy, or multicast, transmission of the payload to multiple destinations being facilitated when multiple destinations are designated by the packet header).**

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the



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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sang et al. in view of Poteet et al. (U.S. Pat. 4630240) and in further view of Bansal et al. (U.S. Pat. 6650637).

**With respect to claim 4**, Sang et al. does not disclose that the multi-port store/switch memory array facilitates double-ended write of incoming packets.

Poteet et al., in the field of communications, discloses the use of double ended write in a memory system (**See column 7 lines 11-18 of Poteet et al. for reference to a dynamic memory including a double-ended write operation**). Using a memory with double ended write has the advantage of allowing for less memory write errors since two write signals must be used to activate the write function.

It would have been obvious to one of ordinary skill in the art at the time of the invention, when presented with the work of Poteet et al., to combine the use of the double-ended write operation of Poteet et al. with the memory and switch of Sang et al., with the motivation being to allow for less memory write errors since two write signals must be used to activate the write function.

Sang et al. also does not disclose that the multi-port store/switch memory array facilitates buffered multi-port read of outgoing packet payloads.

Bansal et al., in the field of communications, discloses the use of buffered multi-port read of outgoing packet payloads (**See column 3 lines 11-23 of Bansal et al. for reference to the use of a buffered multi-port read operation in a multi-port RAM**). Using a memory with buffered multi-port read has the advantage of allowing multiple

read functions as well as write functions to be carried out during a single memory clock cycle.

It would have been obvious to one of ordinary skill in the art at the time of the invention, when presented with the work of Bansal et al., to combine the use of buffered multi-port read as suggested by Bansal et al. with the memory and switch of Sang et al. and Poteet et al., with the motivation being to allow multiple read functions as well as write functions to be carried out during a single memory clock cycle.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sang et al. in view of Majos et al. (U.S. Pat. 5640366).

**With respect to claim 5**, Sang et al. does not disclose that the multi-port store/switch memory array facilitates double port write of incoming packets and buffered double port read of outgoing packets.

Majos et al., in the field of communications, discloses a memory using double port write and double port read (**See column 5 lines 22-35 of Majos et al. for reference to a double port random access memory with both double port write and double port read operations**). Using a memory with double port read and double port write has the advantage of allowing multiple read functions as well as write functions to be carried out during a single memory clock cycle.

It would have been obvious to one of ordinary skill in the art at the time of the invention, when presented with the work of Majos et al., to combine the use of double port write and read functions as suggested by Majos et al. with the memory and switch

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of Sang et al., with the motivation being to allow multiple read functions as well as write functions to be carried out during a single memory clock cycle.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sang (U.S. Pat. 6724769) discloses a switch with a separate memory for each MAC data port. Soman et al. (U.S. Pat. 6138219) discloses a multi-port memory array similar to the one used in the switch of the present application. Conlin et al. (U.S. Pat. 6212597) discloses a multi-port memory that can be used to multicast data directly to multiple destination ports.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E Mattis whose telephone number is (703) 305-8702. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jem

A handwritten signature in black ink, appearing to read 'Huy D. Vu', is written over a horizontal line.

HUY D. VU  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600